ROS2/DDSのプロトコルで FPGAが PUBLISH/SUBSCRIBE 通信する ものをつくるプロジェクト

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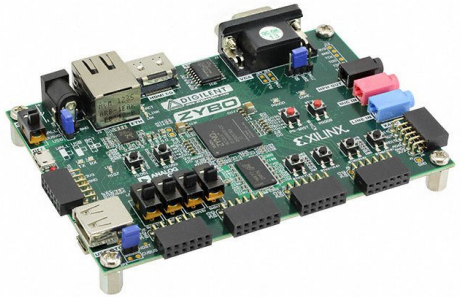
ARM **搭載**FPGA：Zynq(Xilinx) or FPGA-SoC(Intel)

- ROS2 on Zybo
  - Xilinx Zynq搭載の小型基板



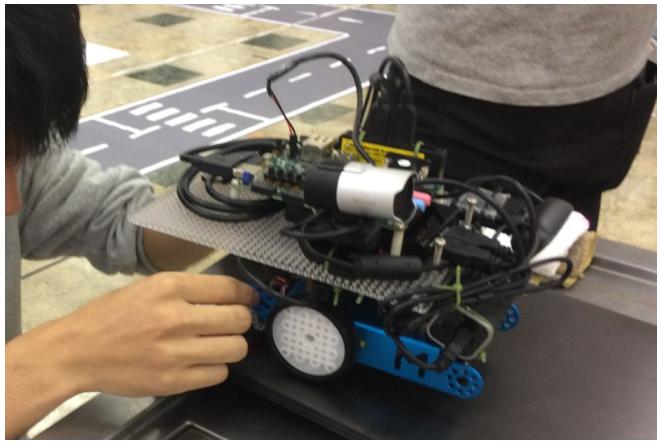
- FPGA acceleration of ROS2 Security
  - Communication by hardwired UDP/IP (DDS, ROS2)
  - Wire-speed data encryption
  - Combined with image processing/DNN

ROS2 on Zybo

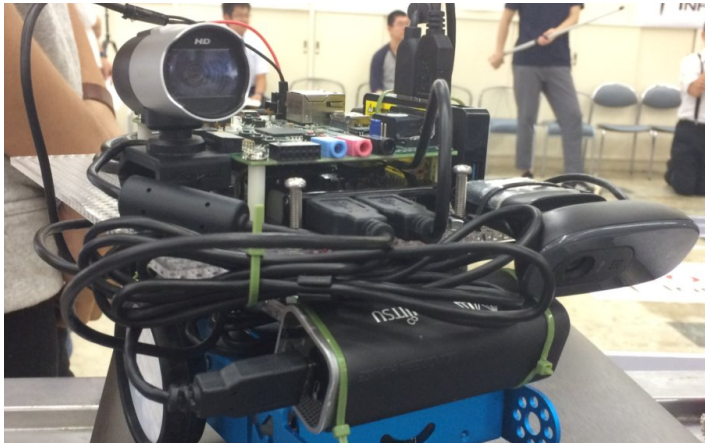

Takeshi Ohkawa
@TakeshiOhkawa
UGOITA! (ROS2 on Zybo)
ツイートを翻訳
192.168.10.18 - ohkawa@localhost: ~/ros2_ws VT
192.168.10.18 - Tera Term VT
16:38 - 2018年6月11日
4件のリツイート 9件のいいね
4
9

Zybo+mBot

@TakeshiOhkawa



9/9 第８回　相磯秀夫杯
FPGAデザインコンテストに出場(第４位)



Zynq (FPGA+ARM(ROS2))
+
mBot で自動運転

（TurtleBot3にするかも）

ROSの豊富なライブラリやシミュレータを活用
重い処理をFPGAにさせてCPUの負担を軽減
FPT2018 DESIGN COMPETITIONに向けて
開発中

FPT2018 FPGA Design Competition
挑戦者募集中！！

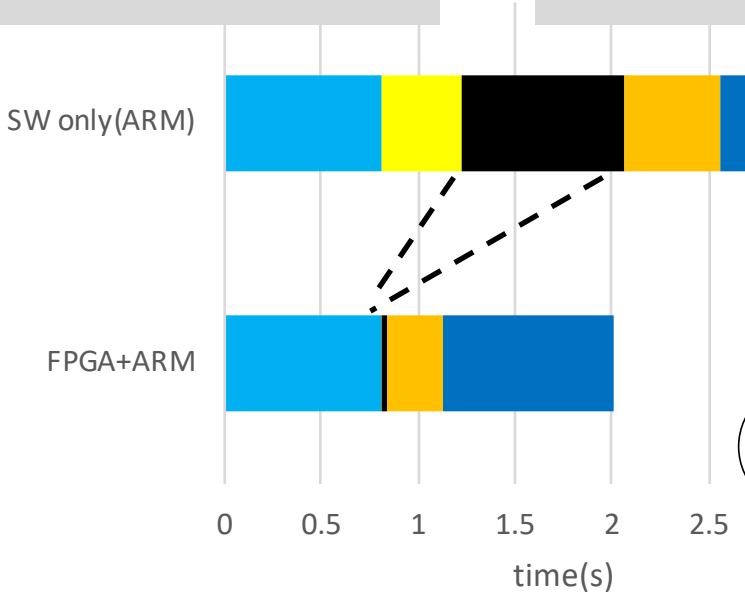
- ENTRY Due: 09/15 (AOE)
- Paper Submission Due: 09/22
- FPT2018 Registration: 10/06
- CHALLENGE @Naha!!:

December, 2018

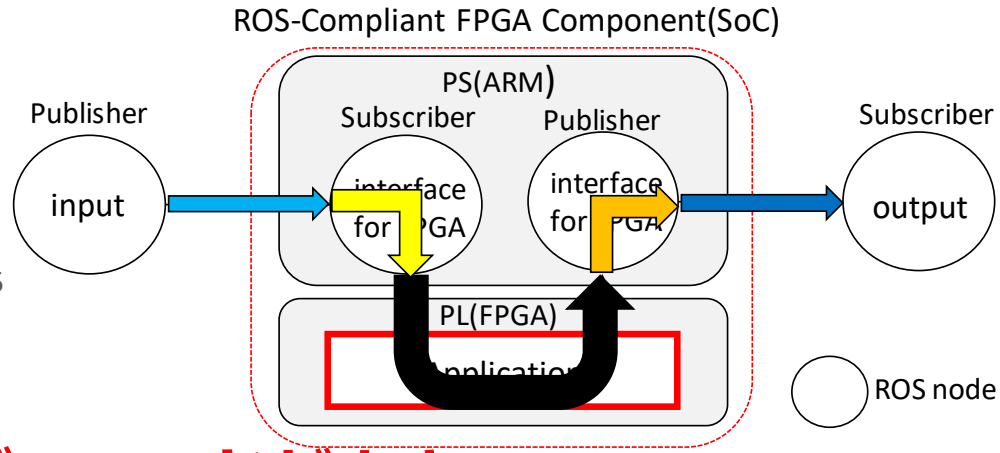
Programmable SoC を使用した ROS準拠FPGAコンポーネントの課題 (ROSCon2017@Vancouverで発表)

Speed UP 1.7x

Speed UP 26x



Resolution：1920 x 1080
Zedboard (Zynq-7020)
ARM(PS): Cortex-A9 666MHz
FPGA(PL): 100MHz

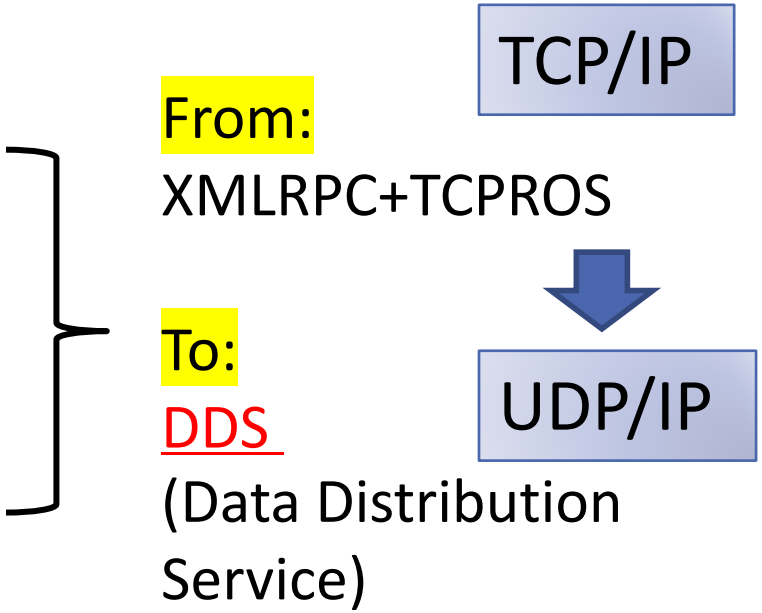


Problem: TCP/IPの通信オーバーヘッドが大きい

Kazushi Yamashina, Takeshi Ohkawa, Kanemitsu Ootsu and Takashi Yokota : “Proposal of ROS-compliant FPGA Component for Low- Power Robotic Systems - case study on image processing application -”, Proceedings of 2nd International Workshop on FPGAs for Software Programmers, FSP2015, pp. 62-67, 2015.

Why ROS2? Brian Gerkey says:

- Teams of multiple robots
- Small embedded platforms
- Real-time systems
- Non-ideal networks
- Production environments
- Prescribed patterns for building and structuring systems



https://design.ros2.org/articles/why_ros2.html

ROS2/DDS の通信内容分析環境

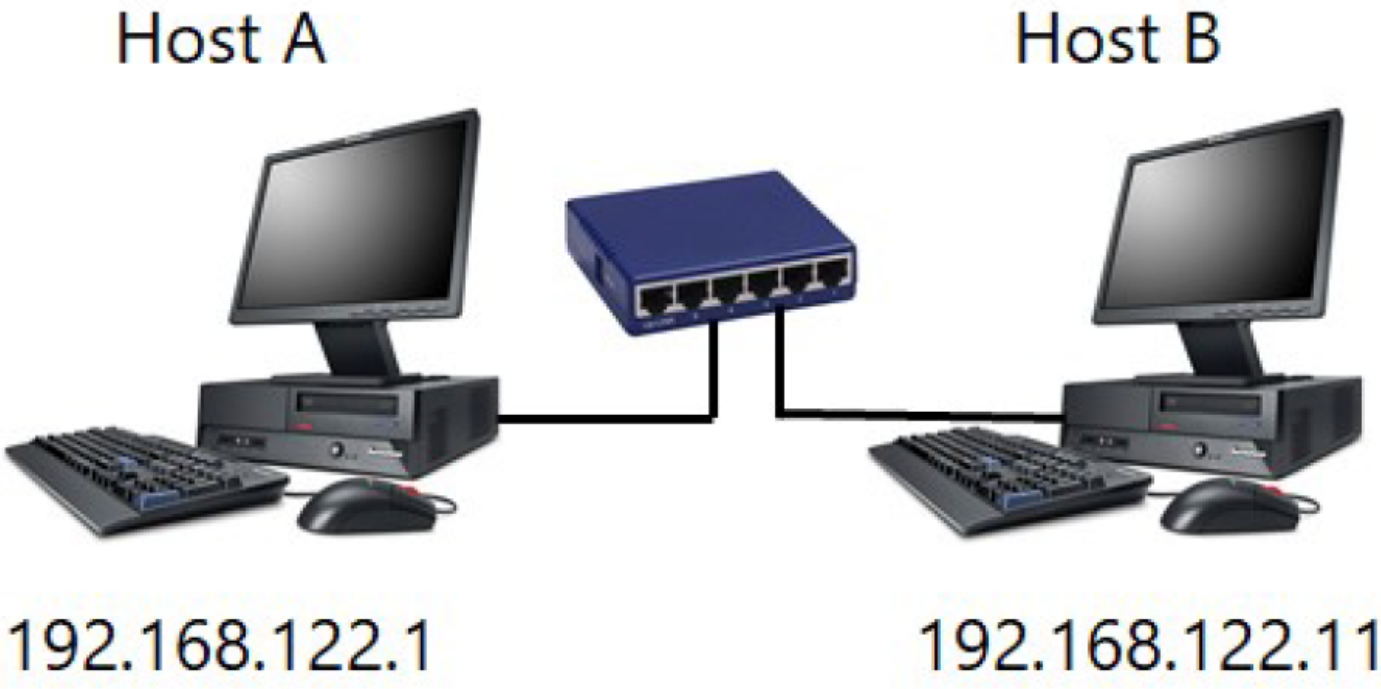


図 1 ROS2/DDS 通信測定環境の構成

パケットキャプチャ結果（Wireshark）

```
126 52.39662 192.168.122.115 192.168.122.1   RTPS    138 INFO_DST, INFO_TS, DATA
127 53.39691 192.168.122.115 192.168.10.143  RTPS    138 INFO_DST, INFO_TS, DATA
128 53.39694 192.168.122.115 192.168.122.1   RTPS    138 INFO_DST, INFO_TS, DATA
129 54.38953 192.168.122.1   192.168.122.115 RTPS    110 INFO_DST, HEARTBEAT
130 54.38961 192.168.122.1   239.255.0.1     RTPS    110 INFO_DST, HEARTBEAT
131 54.38964 192.168.122.1   192.168.122.115 RTPS    110 INFO_DST, HEARTBEAT
132 54.38968 192.168.122.1   239.255.0.1     RTPS    110 INFO_DST, HEARTBEAT
133 54.38972 192.168.122.1   192.168.122.115 RTPS    110 INFO_DST, HEARTBEAT

Frame 126: 138 bytes on wire (1104 bits), 138 bytes captured (1104 bits) on interface 0
Ethernet II, Src: RealtekU_26:a6:ae (52:54:00:26:a6:ae), Dst: fe:54:00:26:a6:ae (fe:54:00:26:a6:ae)
Internet Protocol Version 4, Src: 192.168.122.115 (192.168.122.115), Dst: 192.168.122.1 (192.168.122.1)
User Datagram Protocol, Src Port: 54951 (54951), Dst Port: 7411 (7411)
Real-Time Publish-Subscribe Wire Protocol

0000  fe 54 00 26 a6 ae 52 54  00 26 a6 ae 08 00 45 00   .T.&..RT .&....E.
0010  00 7c be 3c 40 00 40 11  06 6f c0 a8 7a 73 c0 a8   .|.<@.@. .o..zs..
0020  7a 01 d6 a7 1c f3 00 68  76 3f 52 54 50 53 02 01   z......h v?RTPS..
0030  01 0f 01 0f 7a 73 98 11  00 00 00 00 00 00 0e 01   ....zs.. ........
0040  0c 00 01 0f 0a 8f 10 56  00 00 00 00 00 00 09 01   .......V ........
0050  08 00 ec e2 18 5b 68 1d  55 61 15 05 2c 00 00 00   .....[h. Ua..,...
0060  10 00 00 00 0e 04 00 00  0e 03 00 00 00 00 01 00   ........ ........
0070  00 00 00 01 00 00 0f 00  00 00 48 65 6c 6c 6f 20   ........ ..Hello
0080  57 6f 72 6c 64 3a 20 31  00 00                     World: 1 ..
```

図 2　キャプチャされた RTPS パケットの例

募集

- FPGA x ROS(ROS2)に興味のあるかた
- ROS2/DDSの通信プロトコルに詳しい方
- @TakeshiOhkawaまで